Karunya University
(Karunya Institute of Technology and Sciences)
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1965)

End Semester Examinations - 2015-16 Even Semester - May 2016

14EC2069 VLSI Design

Set B

Time : 3 hrs
Total Marks: 100

1. (i) Explain in detail about IC design process. (12)

   (ii) Discuss in detail about Standard Cell design. (8)

OR

2. i) Explain the different types of semi custom design. (14)

   (ii) With neat diagram discuss about twin-tub CMOS process. (6)

3. (i) Derive the expression for drain current in cutoff, non saturated and saturated region. (14)

   (ii) Draw the circuit, stick diagram and the layout of CMOS inverter. (6)

OR

4. (i)Draw the circuit, stick diagram and the layout of 2-input CMOS NAND Gate.(8)

   (ii)With small signal model for an MOS transistor derive the small signal AC characteristics. (12)

5. (i)With neat diagram explain in detail about NMOS design rules and draw the stick diagram for 2-input NAND using NMOS logic. (14)

   ii)Draw **complementary CMOS logic and pseudo NMOS logic**, for the function and compare the number of transistors. (6)

   $F = \overline{D + A \cdot (B + C)}$

OR

6. (i)Explain in detail about pseudo NMOS logic and draw 3-input NAND gate using pseudo NMOS logic. (14)

   (ii)Draw colour coding representation of various layers in stick diagram and layout in CMOS process. (6)

7. (i)Explain in detail about pseudo NMOS logic and draw 3-input NOR gate using pseudo NMOS logic. (14)

   (ii)Draw the circuit, stick diagram of NMOS 2-input NOR Gate.(6)

OR

8. (i) Explain in detail about NMOS design rules.10)

   (ii) Explain in detail about **n-p CMOS Logic** and draw the following function using C^2MOS Logic.(10)

   $Z=\overline{A.B+C.D}$

9. (i) Explain in detail about CMOS Domino logic and draw the following expression using the same. (10)

   $Z = AB + (C + D)(E + F) + GH$

   (ii) Draw 2-input NOR gate using C^2MOS Logic. (5)

   (iii) Write short notes on design rules.(5)

Wishing you All the Best